We are soliciting contributions that discuss circuits and systems solutions addressing multichip interconnection challenges. Example topics of interest for the special issue include (but are not limited to):

- chip-to-chip communication over backplanes, printed circuits boards and low-loss substrates
- die-to-die communication within a package
- stacked-die communication with through-silicon vias, or proximity inductive or capacitive coupling
- optical and wireless interconnect

Papers may include experimental results or extensive simulation results demonstrating the feasibility of a proposed circuit design approach or system architecture and its effectiveness in addressing interconnection challenges. Papers on the analysis, modeling, and optimization of interconnections will also be considered, including those considering test and/or statistical variation issues.

Papers will be reviewed according to the standard peer review process of the IEEE Transactions on Circuits and Systems–Part II. Manuscripts should conform to the standard requirements for IEEE Transactions and should be submitted electronically through the web page of the TCAS-II (http://tcas2.polito.it). Authors should follow the same steps for submission as for regular papers, but during the submission process, please be sure to place the phrase “Multichip Interconnections” before the title of your manuscript whenever prompted on a web form, so that your paper is identifiable as a special issue submission.

Important: Since the IEEE TCAS-II is a journal for rapid publication of express briefs (5-pages maximum length in double-column format), the aim of the special issue is to publish highly-focused, short contributions describing in a concise and precise form the recent advancements in the field of Circuits and Systems Solutions for High Performance Multi-Chip Interconnections. The goal is to produce an issue bringing to the readership the same excitement as from the participation of a focused special session in the most prestigious conference in the area.

**Guest Editor:**
Prof. Vladimir M. Stojanovic  
Department of Electrical Engineering and Computer Science, M.I.T., Cambridge, MA, USA  
Email: vlada@mit.edu

Prof. C.-K. Ken Yang  
Electrical Engineering Department, University of California-Los Angeles, Los Angeles, CA, USA  
Email: yang@ee.ucla.edu

Dr. Ron Ho  
VLSI Research Group, Sun Microsystems Research Labs, Menlo Park, CA, USA  
Email: ron.ho@sun.com

**Deadlines:**
- Manuscript submission: **Oct 30 2009** [Extended]  
- Notification of acceptance: Jan 10 2010  
- Final manuscript submission: Feb 10 2010  
- Tentative publication date: Apr 2010